IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.- 10. (Cancelled)

11. (Currently Amended) A semiconductor memory element, comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed in said semiconductor substrate between said source region and said drain region;

~~a silicon oxide~~an insulation film arranged on a portion of said semiconductor substrate corresponding to said channel region, wherein a plurality of silicon microcrystal grains are formed in said ~~silicon oxide~~insulation film; and

a gate electrode formed over said ~~silicon oxide film and comprised of a metal or a semiconductor~~ insulation film to control electric potential of said channel region,

wherein a perimeter of each of said silicon microcrystal grains is covered with said ~~silicon oxide~~insulation film so that each of said microcrystal grains constitutes an independent and isolated charge storage region such that said plurality of said charge storage regions are electrically disconnected, and

wherein an electric potential to be applied to said gate electrode upon writing of data and an electric potential to be applied to said gate electrode upon erasing of data have the same polarity.

12. (Cancelled)

13. (Previously Presented) A semiconductor memory element according to claim 11,

wherein said plurality of microcrystal grains have a mean size of approximately 10 nm.

14. (Cancelled)

15. (Previously Presented) A semiconductor memory element according to claim 11,

wherein said plurality of charge storage regions store charges from the same bit of data.

16. (Cancelled)

17. (Currently Amended) A semiconductor memory element, comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed in said semiconductor substrate between said source region and said drain region;

~~a silicon oxide~~an insulation film arranged on a portion of said semiconductor substrate corresponding to said channel region; and

a gate electrode formed over said ~~silicon oxide~~insulation film ~~and comprised of a metal or semiconductor~~ to control electrical potential of said channel region,

wherein said ~~silicon oxide~~insulation film includes means for dispersing charges corresponding to one bit of data written into said semiconductor element into a plurality of independent isolated charge storage regions, and

wherein an electric potential to be applied to said gate electrode upon writing of data and an electric potential to be applied to said gate electrode upon erasing of data have the same polarity.

18. (Currently Amended) A semiconductor memory element according to claim 17,

wherein said means for dispersing charges includes a plurality of silicon microcrystal grains formed in said insulation film which are electrically disconnected from one another.

19. (Previously Presented) A semiconductor memory element according to claim 18,

wherein said plurality of microcrystal grains have a mean size of approximately 10 nm.

20. (Cancelled)

21. (New) A semiconductor memory element according to claim 11, wherein said insulation film is comprised of silicon oxide.

22. (New) A semiconductor memory element according to claim 17, wherein said insulation film is comprised of silicon oxide.

23. (New) A semiconductor memory element according to claim 11, wherein said gate electrode is comprised of a metal or a semiconductor.

24. (New) A semiconductor memory element according to claim 17, wherein said gate electrode is comprised of a metal or a semiconductor.

25. (New) A semiconductor memory element, comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed in said semiconductor substrate between said source region and said drain region;

an insulation film arranged on a portion of said semiconductor substrate corresponding to said channel region; and

a gate electrode formed over said insulation film to control electrical potential of said channel region,

wherein said insulation film includes means for dispersing charges corresponding to one bit of data written into said semiconductor element into a plurality of independent isolated charge storage regions, and

means for permitting writing of data and erasing of data to and from said independent isolated charge storage regions by applying a first electric potential to

said gate electrode for writing of data and applying a second electric potential to said gate electrode for erasing of data, wherein said first and second electric potentials each have the same polarity.

Claim 26. (New) A semiconductor memory element according to claim 25, wherein said means for dispersing changes and permitting writing and erasing of data includes a plurality of silicon microcrystal grains formed in said insulation film which are electrically disconnected from one another, such that said insulation film separates said silicon microcrystal grains from each other and from both the substrate and the gate electrode.

Claim 27. (New) A semiconductor memory element according to claim 26, wherein said plurality of microcrystal grains have a mean size of approximately 10 nm.